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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,967	11/27/2001	Takashi Yamada	P 28403201F171	8085

7590 06/17/2004

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EXAMINER	
LEWIS, MONICA	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,967	YAMADA ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 21-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 21-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the request for continued examination filed April 6, 2004.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/6/04 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 1-8 and 21-28 have been considered but are moot in view of the new ground(s) of rejection.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "increased width portion of said groove is formed to cover an entire range of a thickness of said dielectric film" must be shown or the feature(s) canceled from the claim(s) (See Claim 5). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures

appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-8 and 21-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "only said bottom surface in a whole surface of said semiconductor layer" (See Claims 1 and 21). Claims 2-8 and 22-28 depend directly or indirectly from a rejected claim and are, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3, 6, 21, 24, 27 and 28, as far as understood, are rejected under 35 U.S.C. 103(a) as obvious over Radens et al. (U.S. Patent No. 6,426,252).

In regards to claim 1, Radens et al. ("Radens") discloses the following:

a) an element substrate (124) including a semiconductor layer of a first conductivity type being insulatively formed over a semiconductor substrate (126) with a dielectric film (122) interposed there between and such that said dielectric film is in contact with said semiconductor substrate (For example: See Figure 2B);

b) element substrate having a groove formed therein with a depth extending from a top surface of said semiconductor layer into said dielectric film, said groove in said dielectric film, being receded laterally as to expose a bottom surface of said semiconductor layer and such that the width of said groove in said dielectric film is greater than that of said groove in said semiconductor layer (For Example: See Figures 2C);

c) an impurity diffusion source (144) buried in said laterally receded portion of said groove to be contacted with only said bottom surface in a whole surface of said semiconductor layer (For Example: See Figure 2D); and

d) a transistor having a first diffusion layer (162) of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer (160) of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode (154) formed at a side face of said groove over said impurity diffusion source with a gate insulation film (152) between said side face and said gate electrode (For Example; See Figure 2H).

In regards to claim 1, Radens discloses the following:

Although Raden does not specifically disclose the conductivity type, it is disclosed that the preferred embodiment disclosed is for example only and not intended as a limitation. Additionally, it is stated that a person of ordinary skill would understand how to replace n-type dopant with p-type dopant (For Example: See Column 5 Lines 17-25).

Additionally, the following limitation makes it a product by process claim: a) "being formed through impurity diffusion" and "formed through impurity diffusion." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 2, Radens discloses the following:

a) groove is formed deep enough to reach the inside of said semiconductor substrate after penetration through said dielectric film (For Example: See Figures 2A); and

b) a trench capacitor formed under said dielectric film to have a storage electrode (134) as half buried in said groove, for constitution of a DRAM cell together with said transistor (For Example: See Figure 2I).

In regards to claim 3, Radens discloses the following:

a) a buried strap for use as said impurity diffusion source is formed in said laterally receded portion and buried in said groove portion overlying said storage electrode to be contacted with said semiconductor layer only at the bottom surface thereof, and wherein this buried strap is covered with a cap insulation film (148) with the gate electrode of said transistor embedded to overlie said cap insulation film (For Example: See 2H).

In regards to claims 6 and 24, Radens discloses the following:

a) semiconductor layer is partitioned into a plurality of element regions by an element isolating insulative film (156) formed and buried deep enough to reach said dielectric film while letting two DRAM cells be disposed at opposite end portions of each said element region word line (158) connected to the gate electrode of said transistor and a bit line (166) coupled (164) to the second diffusion layer of said transistor said word line and said bit line being continuously disposed to cross each other (For Example: See Figure 2I and Figure 3).

In regards to claim 21, Radens discloses the following:

a) an element substrate including a semiconductor layer of a first conductivity type being insulatively formed over a semiconductor substrate with a dielectric film interposed there between and such that said dielectric film is in contact with said semiconductor substrate (For example: See Figure 2B);

b) element substrate having a groove formed therein with a depth extending from a top surface of said semiconductor layer into said dielectric film, said groove in said dielectric film, being receded laterally as to expose a bottom surface of said semiconductor layer and such that the width of said groove in said dielectric film is greater than that of said groove in said semiconductor layer (For Example: See Figures 2C);

c) a trench capacitor formed under said dielectric film to have a storage electrode (134) as half buried in said groove (For Example: See Figure 2I);

d) an impurity diffusion source buried in said laterally receded portion of said groove to be contacted with said bottom surface and top surface of said impurity diffusion source being contacted with said storage electrode and only said bottom surface in a whole surface of said semiconductor layer (For Example: See Figure 2D);

e) a cap insulation film formed in said groove to cover said impurity diffusion source (For Example: See 2H)

d) a transistor having a first diffusion layer (162) of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer (160) of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode (154) formed at a side face of said groove over said impurity diffusion source with a gate insulation film (152) between said side face and said gate electrode (For Example; See Figure 2H).

In regards to claim 21, Radens discloses the following:

Although Raden does not specifically disclose the conductivity type, it is disclosed that the preferred embodiment disclosed is for example only and not intended as a limitation. Additionally, it is stated that a person of ordinary skill would understand how to replace n-type dopant with p-type dopant (For Example: See Column 5 Lines 17-25).

Additionally, the following limitation makes it a product by process claim: a) "being formed through impurity diffusion" and "formed through impurity diffusion." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claims 27 and 28, Radens discloses the following:

a) element substrate is a silicon-on-insulator substrate (For Example: See Figure 2I).

Allowable Subject Matter

10. Claims 4, 5, 7, 8, 22, 23, 25 and 26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final

communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

June 12, 2004

Mary Wilczewski
Primary Examiner